



Advanced Program

ICSJ2010

The Leading International Symposium on Components, Packaging, and Manufacturing Technology

IEEE CPMT Symposium Japan

(Formerly "VLSI Packaging Workshop in Japan")

Aug. 24-26, 2010

The University of Tokyo, Hongo Campus

Faculty of Engineering Bldg.2

Sanjo Conference Hall

The VLSI Packaging Workshop in Japan has been held every two years since 1992 in Kyoto, and it has become a well-known international workshop for advanced packaging technologies. Due to ever increasing activities and changing demands, the committee has reviewed its mission; cooperated with the members of IEEE CPMT Japan Chapter, refurbished the workshop, and started the new symposium - IEEE CPMT Symposium Japan. It will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. The committee strongly encourages you to attend this symposium and participate in the discussion, to understand the technology trends and find the best targets for your technology / business development. Bring your latest research results and share with the participants who are experts from the industry and the grove of Academe, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium.

Features of this symposium are:

- ✓ Fully supported by IEEE CPMT society and wonderful plenary speakers
- ✓ Papers presented in the Symposium will be posted on IEEE Xplore.
- ✓ Special offer 50% off of IEEE and CPMT Society membership
- ✓ Second day focuses on 3D integration and Interconnection
- ✓ Third day focuses on Materials and Optoelectronics

Welcome to IEEE CPMT Symposium Japan

On behalf of the committee of IEEE CPMT Symposium Japan, it is our pleasure to welcome you to this Symposium. This Symposium has been held as IEEE VLSI Package Workshop in Japan every other year since 1992 and is the tenth anniversary this year. To meet the needs of the times, the Workshop has been transformed to IEEE CPMT Symposium Japan by the joint effort of IEEE CPMT society Japan chapter and the organizing committee. We wish to celebrate the new start of the IEEE CPMT Symposium Japan as well as the tenth anniversary of the Workshop. This Symposium is now fully supported by IEEE CPMT society and technically supported by National Institute of Advanced Industrial Science and Technology (AIST).

With the strong support of IEEE CPMT Society, we have invited distinguished researchers from all over the world as plenary speakers, especially on the rapidly emerging packaging technology from fundamentals to applications and from nano level to system level. We would like to express our gratitude to all authors and invited speakers for presenting their latest research results, and all participants for their active cooperation.

Our mission is to offer the opportunity to the people who wish to extend their R&D activity beyond borders to exchange technical knowledge and perspective. We will convey your names across the world via IEEE Xplorer, which is the most powerful on-line archive of papers under the academic authority. Each of our committee members will do our best so that you will reap a rich harvest from this Symposium.

August 24th, 2010

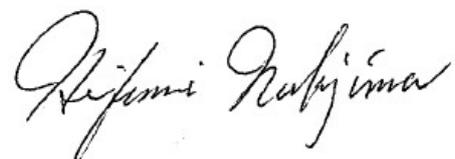
Tokyo, Japan



Tadatomo Suga, ICSJ General Chair



Masahiro Aoyagi, IEEE CPMT Society Japan Chapter Chair



Hirofumi Nakajima, Organizing Committee, Executive Chair

Preceding-day event

August 23, 2010

	Room 212
9:00	ITRS Workshop <i>(No registration required)</i> <i>ITRS Assembly and packaging workshop steered by W. R. Bottoms and William Chen</i> <i>ITRS and Jisso Roadmap activity: Difficult challenges in packaging technology</i>
17:00	Adjourn

Symposium Schedule

August 24, 2010

8:30	Registration		
	Room 213		
9:30	Opening Remarks: <i>Hirofumi Nakajima , Executive Chair, IEEE CPMT Symposium Japan; Renesas Electronics Co.</i>		
9:40	Welcome Talk CPMT President: <i>Rolf Aschenbrenner, President, CPMT Society, IEEE; Fraunhofer IZM</i>		
9:50	Plenary Speech : <i>William T. Chen (Senior Technical Advisor ASE Group, IEEE/CPMT Society Distinguished Lecturer)</i>		
10:35	<i>Coffee break</i>		
10:45	Plenary Speech : <i>W. R. Bottoms (Chair, A&P TWG, ITRS; Chairman, 3MTS)</i>		
11:30	Plenary Speech : <i>C. P. Wong (Dean of the Faculty of Engineering, The Chinese University of Hong Kong, On a no pay leave from School of Materials Science and Engineering, Georgia Institute of Technology, IEEE/CPMT Society Distinguished Lecturer)</i>		
12:10	<i>Lunch</i>		
	Room 213	Room 212	Room 211
13:00	Session 1: Advanced Package - 1	Session 3: Board Level Reliability -1	Session 5: Electrical Design -1
14:40	Author's Interview	Author's Interview	Author's Interview
15:00	<i>Coffee break</i>		
15:10	Session 2: Advanced Package - 2	Session 4: Board Level Reliability -2	Session 6: Electrical Design -2
16:50	Author's Interview	Author's Interview	Author's Interview
17:20	Welcome Reception (Sanjo Conference Hall)		
20:00	<i>Close</i>		

August 25, 2010

9:00	Registration		
	Room 213		
9:30	Plenary Speech : <i>Tadatomo Suga (General Chair, IEEE CPMT Symposium Japan; The University of Tokyo)</i>		
10:20	<i>Coffee break</i>		
10:30	Plenary Speech : <i>Klaus-Dieter Lang (Fraunhofer IZM)</i>		
11:15	Plenary Speech : <i>Eric Beyne (IMEC)</i>		
12:00	<i>Lunch</i>		
	Room 212	Room 213	Room 211
13:00	Session 7: Interconnect	Session 9: 3D Integration - 1	Session 11: Mechanical Design -1
14:40	Author's Interview	Author's Interview	Author's Interview
15:00	<i>Coffee break</i>		
15:10	Session 8: Optical vs. Electrical Transmission	Session 10: 3D Integration -2	Session 12: Mechanical Design -2
16:50	Author's Interview	Author's Interview	Author's Interview
17:10	Close		

August 26, 2010

9:00	Registration		
	Room 213		
9:30	Plenary Speech : <i>E. Jan Vardaman (President, TechSearch International, Inc.)</i>		
10:15	Plenary Speech : <i>Masahiro Aoyagi (Chair, CPMT Society Japan Chapter; AIST)</i>		
11:00	<i>Coffee break</i>		
	Room 212	Room 213	Room 211
11:10	Session 13: Thermal Design -1	Session 15: Material - 1	Session 18: Optoelectronics -1
12:00	Author's Interview	Author's Interview	Author's Interview
12:10	<i>Lunch</i>		
13:00	Award ceremony (Room 213)		
13:20	Session 14: Thermal Design - 2	Session 16: Material - 2	Session 19: Optoelectronics - 2
15:00	Author's Interview	Author's Interview	Author's Interview
15:20	<i>Coffee break</i>		
15:30		Session 17: Material -3	Session 20: Optoelectronics - 3
17:10		Author's Interview	Author's Interview
17:30	Close		

Plenary Speech

August 24, 2010, Room 213

Session Chair: Hirofumi Nakajima

9:50		<p>Materials – Crucial Enabler for Packaging Innovation, <i>William T. Chen (Senior Technical Advisor ASE Group, IEEE/CPMT Society Distinguished Lecturer)</i></p>
<p>The last decade has seen great advances in packaging technology with new package types, lower cost innovations, miniaturizations and integration. They are driven by the dual forces of market pull (Consumer electronics, mobile devices, and networking everywhere) and technology push (More Moore and More than Moore). Behind the scene new materials and new materials processing have played a crucial enabling role. In the ITRS report it has been stated that in the last decade 100% of the materials have been replaced, and that this pace of change have not slackened. This talk will present advances in packaging technologies and the role of materials and materials processing innovations. We will illustrate with some of the leading consumer applications. We will discuss what we may expect to see in the next decade for this exemplary and productive collaboration in the electronics ecosystem.</p>		
10:45		<p>Difficult Challenges and potential solutions for Advanced Packaging, <i>W. R. Bottoms (Chair, A&P TWG, ITRS; Chairman, Third Millennium Test Solutions)</i></p>
<p>The driving forces for the electronics industry will be increasingly dominated by consumer demands over the 15 year view of the International Technology Roadmap for Semiconductors (ITRS). The resulting difficult challenges in advanced packaging will arise from thermal management, size, power, bandwidth density and cost requirements. We have known solutions for many of the technical requirements today but many of these solutions do not meet the size and cost requirements of the ITRS Roadmap. These challenges cannot be met without the incorporation of new materials, new processes and new architectures. The most important of these is 3D integration. Although there has been significant progress in development of 3D technologies it has not yet reached the high volume production mainstream. Recent progress such as the advent of 3D standards will result in the emergence of high volume 3D IC production this year for less complex products. The major driving issues and challenges associated with 3D IC production and the outlook for future 3D integration of more complex products will be discussed.</p>		

11:30		<p>Recent Advances on Nano-materials for Advanced Packaging Applications, <i>C. P. Wong (Dean of the Faculty of Engineering, The Chinese University of Hong Kong, On a no pay leave from School of Materials Science and Engineering, Georgia Institute of Technology, IEEE/CPMT Society Distinguished Lecturer)</i></p>
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The advance of semiconductor technology is mainly due to the advances of materials, especially polymeric materials. These include the use of polymers as: resist (for deep submicron lithography), adhesives (both conductive and non conductive for die attach and assembly interconnects), interlayer dielectrics (low k, low loss dielectrics for high speed and low loss signal transmission), encapsulants (discrete and wafer level packages for device protection), embedded passives (high K, capacitors, high Q, inductors for high density PWB substrates), superhydrophobic self-cleaning lotus effect surfaces, ...etc. In this presentation, I will review some of the recent advances on polymeric materials and polymer nanocomposites that are currently being investigated for these types of applications, such as : lead-free electrically conductive adhesives (ECAs) with self assembly monolayer molecular wires for fine pitch and high current density interconnects, flip chip and wafer level underfills, nano lead-free alloys for low temperature interconnects, nanometal particle composites for high k embedded passives, well-aligned carbon nanotubes and graphenes for high current and high thermal interface materials (TIMs), and superhydrophobic self-clean lotus surface coatings for high efficiency solar cell applications.

August 25, 2010, Room 213

Session Chair: Ricky Lee

9:30		<p>Recent Progress in Surface Activated Bonding Method, <i>Tadatomo Suga (General Chair, IEEE CPMT Symposium Japan; School of Engineering of The University of Tokyo)</i></p>
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10:30		<p>3D System-in-Package Technologies for Multifunctional Systems, <i>Klaus-Dieter Lang (Fraunhofer IZM)</i></p>
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Semiconductor roadmaps predict that the advancement in silicon technologies will follow the well known "Moore's law" in the next decade, too. However, for future multifunctional systems in many cases the cost efficient IC standard technologies cannot be applied. Non-digital and often MEMS functions require alternative materials, specific assembly processes and application environment oriented packaging solutions.

Therefore future system integration often will be a combination of "More Moore" - or "system on chip (SoC)"-solutions and advanced assembly and packaging technologies, for example "system in package (SiP)" or "system on board (SoB)". Main advantages of these approaches are performance improvement and application flexibility for different product groups, manufacturability with established processes and a high potential for cost reduction.

From the technological perspective 3D waferlevel and 3D module assembly and packaging technologies as well as the embedding of active and passive components in polymeric substrates are promising approaches in this context.

The presentation describes the strategy as well as advantages and disadvantages concerning advanced 3D packaging solutions at wafer and module level. Technology background, implementation conditions and exploitation experiences as well as application examples will be presented.

11:15



3D System Integration - Opportunities and challenges in the supply chain, *Eric Beyne (IMEC)*

3D integration complements semiconductor scaling; it enables a higher integration density as well as heterogeneous technology integration. Using 3D chip stacking, it is possible to extend the number of functions per 3D chip well beyond the near-term capabilities of traditional scaling. The 3D strata may be realized using advanced CMOS technology nodes but may also exploit a wide variety of device technologies to optimize system performance.

The study and development of 3D System integration requires a concurrent exploration of technology and design issues with a target to a specific 3D application domain.

The introduction of 3D technology in the microelectronic industry calls for innovations throughout the supply chain. The technology needed for 3D stacking consists of three main processes: The through-Si via process, processes for bonding and thinning wafers on carriers, allowing for backside processing on thinned wafers, and the actual chip stacking and stack packaging operations. Next to the technology, the design of 3D systems is a key topic of the 3D research program. 3D system design exploration

August 26, 2010, Room 213

Session Chair: Hiroshi Yamada

9:30		3D Packaging Trends: From Stacked Die to 3D ICs with TSV <i>E. Jan Vardaman (President, TechSearch International, Inc.)</i>
10:15		Advanced Electrical Measurement and Evaluation Technology for 3D LSI Chip Stacking Integration Technology, <i>Masahiro Aoyagi (Chair, CPMT Society Japan Chapter; The National Institute of Advanced Industrial Science and Technology)</i>
<p>3D LSI chip stacking technology is one of key technologies for future high density electronic system integration. Its process technology are established gradually. However, its measurement and evaluation technology is not developed well compared to the process technology. In AIST, high resolution TDR/TDT measurement, ultra-wide band power distribution network impedance measurement technologies have been developed intensively as an advanced electrical measurement technology.</p> <p>The details of these technologies will be introduced.</p>		

Program Sessions

August 24, 2010

Room 213

13:00 – 14:40 Session 1: Advanced Package (AP-1)

Session Chair: Shoji Uegaki, Klaus Pressel

- 1-1 **Module Miniaturization by ultra thin Package Stacking,**
Thomas Löher¹, David Schütze¹, Andreas Ostmann² and Rolf Aschenbrenner² / Technische Universität Berlin¹, Fraunhofer IZM²
- 1-2 **Development of Super Thin TSV PoP,**
Flynn Carson¹, Kazuo Ishibashi², Seung Wook Yoon³, Pandi Chelvam Marimuthu³ and Dzafir Shariff³ / STATS ChipPAC, Inc.¹, Nokia Japan Co., Ltd.², STATS ChipPAC Singapore, Ltd.³
- 1-3 **A wafer-level system integration technology for flexible pseudo-SOC incorporates MEMS-CMOS heterogeneous devices,**
Hiroshi Yamada¹, Yutaka Onozuka¹, Atsuko Iida¹, Kazuhiko Itaya¹, Hideyuki Funaki¹, Kazuhiro Takahashi² and Hiroshi Toshiyoshi², / Toshiba Corporation¹, The University of Tokyo²
- 1-4 **Silicon TSV Interposer with embedded capacitors for high performance VLSI packaging,**
Nagesh Vodrahall / Allvia Technologies

Author's Interview (20min.)

15:10 – 16:50 Session 2: Advanced Package (AP-2)

Session Chair: Shigenori Aoki, C.P. Hung

- 2-1 **Alternative Process and Support Material for Embedded Fine-pad-pitch LSI Package,**
Hideya Murai, Kentaro Mori, Masaya Kawano and Shintaro Yamamichi / Renesas Electronics Corporation
- 2-2 **Preparation of ferroelectric capacitor films onto the releasable substrate and its application to nano-transfer method,**
Masaaki Ichiki^{1,3,4}, Keita Iimura¹, Toshifumi Hosono¹, Keisuke Kuraki¹, Fumiaki Tomioka¹, Tadatomo Suga^{1,3} Ryutaro Maeda² and Toshihiro Itoh^{2,3} / The University of Tokyo¹, National Institute of Advanced industrial Science and Technology(AIST)², JST-CREST³, JST-PRESTO⁴
- 2-3 **Embedded Wafer Level Ball Grid Array (eWLB) Technology for System Integration,**
Klaus Pressel, Gottfried Beer, Thorsten Meyer, Maciej Wojniwski, Markus Fink, Gerals Ofner and Bernd Römer / Infineon Technologies AG.
- 2-4 **High Density Substrate Solution for Complex High Pin Count Flip-Chip Applications,**
Vern Solberg¹ and Vage Oganessian² / STC-Madison¹, Tessera Technologies, Inc.²

Author's Interview (20min.)

Room 212

13:00 – 14:40 Session 3: Board Level Reliability (BR-1)

Session Chair: Michitaka Kimura, Jie Xue

- 3-1 **Invited : Mechanical and Material Reliability in Board Level Solder Joints,**

Masazumi Amagai / Texas Instruments Japan Ltd.

- 3-2 **Effect of Mild Aging on Package Drop Performance for Lead Free Solders,**
SeokHo Na, SeWoong Cha, WonJoon Kang, TaeSeong Kim, TaeKyung Hwang, JinYoung Khim / Amkor Technology Korea
- 3-3 **Next Generation Substrate for High Density and Thin Package,**
Toru Furuta / IBIDEN CO.,LTD.
- 3-4 **PoP Prototyping by determination of matter transport effects,**
Lutz Meinshausen¹, Kirsten Weide-Zaage¹, Wei Feng² and Hélène Frémont² / Leibniz University Hannover¹, Université Bordeaux P²

Author's Interview (20min.)

15:10 – 16:50 Session 4: Board Level Reliability (BR-2)

Session Chair: Michitaka Kimura, Jie Xue

- 4-1 **Modeling of Board Level Solder Joint Reliability under Mechanical Drop Test with the Consideration of Plastic Strain Hardening of Lead-free Solder,**
Z. J. Xu, T. Jiang, F. B. Song, Jeffery C. C. Lo and S. W. Ricky Lee / Hong Kong University of Science and Technology
- 4-2 **Effect of Solders, Underfills and Substrates on Reliability of Flip-Chip Bonding of Low-k Semiconductor Chips,**
Kenji Terada, Takayuki Nejime, Takafumi Ooyoshi, Kaoru Kobayashi and Kimihiro Yamanaka / KYOCERA SLC Technologies Corporation
- 4-3 **Health monitoring method for load assessment in reliability design of printed circuit board,**
Kenji Hirohata, Katsumi Hisano, Yosuke Hisakuni, Takahiro Omori and Minoru Mukai / Toshiba Corporation
- 4-4 **Effects of the crystallographic orientation of Sn grain during electromigration test,**
Kiju Lee¹, Keun-Soo Kim¹, Kimihiro Yamanaka², Yutaka Tsukada¹, Soichi Kuritan³, Mimoru Ueshima⁴ and Katsuaki Suganuma¹ / Osaka University¹, KYOCERA SLC Technologies Corporation², ESPEC.CORP.³, SENJU METAL INDUSTRY CO.,LTD.⁴

Author's Interview (20min.)

Room 211

13:00 – 14:40 Session 5: Electrical Design (ED-1)

Session Chair: Toshio Sudo, Yutaka Uematsu

- 5-1 **Design Trade-Off for Resonance Reduction of Multiple Power Planes in Super Ball Grid Array (SBGA) Package,**
GaWon Kim¹, SeungJae Lee¹, JiHeon Yu¹, Ozgur Mismar², KiCheol Bae¹, TaeKi Kim¹, Sangwoong Lee¹ and JinYoung Kim¹ / Amkor Technology Korea¹, Amkor Technology Inc.²
- 5-2 **Fast Power Integrity Estimation Method by Use of LSI Power-pin Model,**
Takashi Harada, Masashi Ogawa and Manabu Kusumoto / NEC Corporation
- 5-3 **Modeling and Analysis of Differential Signal Through Silicon Via (TSV) in 3D IC,**
Joohee Kim¹, Jun So Pak¹, Jonghyun Cho¹, Junho Lee², Hyungdong Lee², Kunwoo Park² and Joungho Kim¹ /

Korea Advanced Institute of Science and Technology (KAIST)¹, Hynix Semiconductor Inc.²

- 5-4 **A Stopband Enhanced EBG Power/ground Plane based on Via Location Design,**
Chuen-De Wang and Tzong-Lin Wu / National Taiwan University

Author's Interview (20min.)

15:10 – 16:25 Session 6: Electrical Design (ED-2)

Session Chair: Takashi Harada, Hideki Osaka

- 6-1 **TSV Mutual Inductance Effect on Impedance of 3D Stacked On-Chip PDN with Multi-TSV Connections,**
Jun So Pak¹, Jonghyun Cho¹, Joohee Kim¹, Junho Lee², Hyungdong Lee², Kunwoo Park² and Jounggho Kim¹ / Korea Advanced Institute of Science and Technology (KAIST)¹, Hynix Semiconductor Inc.²
- 6-2 **Through Co-Design to Optimize Power Delivery Distribution System Using Embedded Discrete De-coupling Capacitor,**
Chen-Chao Wang¹, Hung-Hsiang Cheng¹, Chi-Tsung Chiu¹, Chih-Pin Hung¹, Chih-Wen Ku² and Toshihide Kitazawa³ / Advanced Semiconductor Engineering Inc.¹, National Sun Yat-Sen University², Ritsumeikan University³
- 6-3 **Impulse responses of on-chip power supply networks with varying conditions,**
Yutaka Uematsu, Hideki Osaka, Masayoshi Yagyū and Tatsuya Saito / Hitachi Ltd.

Author's Interview (20min.)

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Room 212

13:00 – 14:40 Session 7: Interconnect (IC)

Session Chair: Hirofumi Nakajima, C.P. Hung

- 7-1 **Wire Bonding with Pd-Coated Copper Wire,**
Horst Clauberg¹, Bob Chylak¹, Nelson Wong¹, Johnny Yeung² and Eugen Milke³ / Kulicke & Soffa Ind, Inc.¹, Heraeus Materials Singapore Pte Ltd.², WC Heraeus GmbH³
- 7-2 **Fine Pitch Cu Wire Bonding – As Good As Gold,**
Bernd K. Appelt, William T. Chen, Andy Tseng, and Yi-Shao Lai / ASE Group Inc.
- 7-3 **Study of EMC for Cu bonding wire application,**
Hidetoshi Seki¹, Chen Ping², Hiroshi Nakatake³, Shin-ichi Zenbutsu¹ and Shingo Itoh¹ / SUMITOMO BAKELITE Co., Ltd.¹, SUMITOMO BAKELITE SINGAPORE PTE. Ltd.², S.B. RESEARCH Co., Ltd.³
- 7-4 **Process Design of Self-Replication for Micro Bump Formation,**
Kiyokazu Yasuda / Nagoya University

Author's Interview (20min.)

15:10 – 16:50 Session 8: Optical vs. Electrical Transmission (OE-1)

Session Chair: Kanji Otsuka, Toshio Sudo

- 8-1 **Invited : Potential of Wavelength-Division-Multiplexing Optical-Interconnects for Next-Generation System in Packaging,**

Shogo Ura¹ and Kenji Kintaka² / Kyoto Institute of Technology¹, Association of Super-Advanced Electronics Technology (ASET)²

8-2 **Study on Novel Concept of Transmission Signal Assisted with Evanescent Wave Energy,**

Kaoru Hashimoto, Kazuo Kohno, Yutaka Akiyama, Hisashi Kikuchi and Kanji Otsuka / Meisei University

8-3 **A Feasibility Study of Proximity Interconnect Technology Utilizing Transmission Line Coupling,**

Daisuke Iguchi¹, Yutaka Akiyama², Fumiaki Fujii² and Kanji Otsuka² / Fuji Xerox Co., Ltd.¹, Meisei University²

8-4 **Analysis of On-Board Antenna Modules for the Millimeter-Wave Intra-Connect system,**

Sho Ohashi, Takahiro Takeda, Hirofumi Kawamura, Yasuhiro Okada, Masahiro Uno, Yoshiyuki Akiyama and Kenichi Kawasaki / Sony Corporation

Author's Interview (20min.)

Room 213

13:00 – 14:40 Session 9: 3D Integration (3D-1)

Session Chair: Hiroshi Yamada, Rolf Aschenbrenner

9-1 **Development of high accuracy wafer thinning and pickup technology for thin wafer(die),**

Chuichi Miyazaki^{1,2}, Haruo Shimamoto^{1,2}, Toshihide Uematsu^{1,2}, Yoshiyuki Abe^{1,2}, Kosuke Kitaichi^{1,2}, Tadahiro Morifuji^{1,3} and Shoji Yasunaga^{1,3} / Association of Super-Advanced Electronics Technology (ASET)¹, Renesas Technology Corp.², ROHM Co., Ltd.³

9-2 **Development of High speed Copper CMP Slurry for TSV application based on Friction analysis,**

Jin Amanokura¹, Hiroshi Ono¹ and Kyoko Hombō² / Hitachi Chemical Co., Ltd.¹, Hitachi Ltd.²

9-3 **Evaluation of Surface Microroughness for Surface Activated Bonding,**

Kei Tsukamoto, Eiji Higurashi and Tadatomo Suga / The University of Tokyo

9-4 **Guard-Ring Effect for Through Silicon Via (TSV) Noise Coupling Reduction,**

Jonghyun Cho¹, Kihyun Yoon¹, Jun So Pak¹, Joohee Kim¹, Junho Lee², Hyungdong Lee², Kunwoo Park² and Joungho Kim¹ / Korea Advanced Institute of Science and Technology (KAIST)¹, Hynix Semiconductor Inc.²

Author's Interview (20min.)

15:10 – 16:50 Session 10: 3D Integration (3D-2)

Session Chair: Masahiro Aoyagi, E. Jan Vardaman

10-1 **Development of Multi-Stack Process on Wafer-on-Wafer (WOW),**

Koji Fujimoto^{1,4}, Nobuhide Maeda¹, Hideki Kitada¹, Youngsuk Kim¹, Akihito Kawa², Kazuhisa Ara², Tomoji Nakamura³, Kousuke Suzuki⁴ and Takayuki Ohba¹ / The University of Tokyo¹, DISCO Corporation², Fujitsu Laboratories Ltd.³, Dai Nippon Printing Co., Ltd.⁴

10-2 **Room-temperature Si-Si and Si-SiN wafer bonding,**

Ryuichi Kondou, Chenxi Wang and Tadatomo Suga / The University of Tokyo

10-3 **Thermal Stress Analysis of the 3D Die Stacks with Low-Volume Interconnections,**

Sayuri Kohara, Katsuyuki Sakuma, Yoshikazu Takahashi, Tohoyiro Aoki, Kuniaki Sueoka, Keiji Matsumoto, Paul S. Andry, Cornelia K. Tsang, Edmund J. Sprogis, John U. Knickerbocker and Yasumitsu Orii / IBM Japan, Ltd.

10-4 **Wafer and/or chip bonding adhesives for 3D package,**

Toshihisa Nonaka, Koichi Fujimaru, Akira Shimada, Noboru Asahi, Yoshiko Tatsuta, Hiroyuki Niwa and Yasuko

Author's Interview (20min.)

Room 211

13:00 – 14:40 Session 11: Mechanical Design (MD-1)

Session Chair: Masazumi Amagai, Tadaaki Mimura

- 11-1 **Review on the high temperature warpage measurement using shadow moiré,**
Yong Goo Um and Jin Young Khim / Amkor Technology Korea
- 11-2 **Warpage mechanism of single-sided molded package studied with viscoelastic analysis,**
Yusuke Komoto / NITTO DENKO Corporation
- 11-3 **Vibration test durability on large BGA assemblies: Evaluation of reinforcement techniques,**
Matthieu Berthou^{1,2,3}, Hua Lu⁴, Pascal Retailleau¹, Helene Frémon², Alexandrine Guédon-Gracia², Catherine Jephos-Davennet³, Christopher Bailey⁴ / MBDA France¹, IMS Bordeaux Univ-Bordeaux², DGA CELAR³, The University of Greenwich⁴
- 11-4 **The Development of Cleaving - DBG + CMP process,**
Shinya Takyu, Mika Kiritani, Tetsuya Kuroswa and Noriko Shimizu / Toshiba Corporation Semiconductor Company

Author's Interview (20min.)

15:10 – 16:00 Session 12: Mechanical Design (MD-2)

Session Chair: Masazumi Amagai, Seok-Hwan HUH

- 12-1 **Thermal stress analysis of FCBGA during cooling under reflow process,**
Chihiro J. Uchibori and Michael Lee / Fujitsu Labs, America, Inc.
- 12-2 **Assembly-Stress-Mechanism in Pad Areas of Flip Chip Package on High-k/Metal gate Transistors,**
Yukitoshi Ota, Fumito Itoh, Kazuhiro Ishikawa, Kiyomi Hagihara, Takeshi Matsumoto, Teppei Iwase, Yutaka Itoh and Hiroshige Hirano / Panasonic Corporation

Author's Interview (20min.)

August 26, 2010

Room 211

11:10 – 12:10 Session 13: Thermal Design (TD-1)

Session Chair: Atsushi Nakamura, Kishio Yokouchi

- 13-1 **Heat spreader technology for silicon chip,**
Tomoyuki Kosakabe, Masataka Mochizuki, Koichi Mashiko, Yuji Saito, Fumitoshi Kiyooka, Yasuhiro Horiuchi, Gerald Cabusao and Thang Nguyen / Fujikura Ltd.
- 13-2 **A Study of Thermal Performance for Chip-in-Substrate type LED Package Structure,**
Yen-Fu Su¹, Tuan-Yu Hung¹, Shin-Yueh Yang¹ and Kuo-Ning Chiang² / National Tsing Hua University¹, National Center for High-Performance Computing²

Author's Interview (10min.)

13:20 – 14:35 Session 14: Thermal Design (TD-2)

Session Chair: *Atsushi Nakamura, Kishio Yokouchi*

- 14-1 **Study on the Application of Thermal Interface Materials for Integration of HP-LEDs,**
Jun Wu^{1,2}, Meilin Zhuang², Shuzhi Li², Weiqiao Yang² and Jianhua Zhang¹ / Shanghai University¹, Shanghai Research Center of Solid-state Lighting Engineering and Technology²
- 14-2 **Structure function based thermal resistance & thermal capacitance measurement for semiconductor packages,**
Yafei Luo / Mentor Graphics Japan Co., Ltd.
- 14-3 **Data center energy conservation utilizing heat pipe based ice storage system,**
Gerald Cabusao, Masataka Mochizuki, Koichi Mashiko, Tetsuya Kobayashi, Randeep Singh, Thang Nguyen and Xiao Ping Wu / Fujikura Ltd.

Author's Interview (20min.)

Room 213

11:10 – 12:10 Session 15: Material (ML-1)

Session Chair: *Itsuo Watanabe, William T. Chen*

- 15-1 **Invited : Recent Advance in Anisotropic Conductive Adhesives (ACAs) Materials and Processing Technology,**
Kyung-Wook Paik / Korea Advanced Institute of Science and Technology (KAIST)
- 15-2 **Micro- Solder Precoat Technology by Precoat by Powder Sheet method,**
Kaichi Tsuruta, Takeo Kuramoto, Takeo Saitou and Manabu Muraoka / Senju Metal Industry Co., Ltd.

Author's Interview (10min.)

13:20 – 15:00 Session 16: Material (ML-2)

Session Chair: *Atsushi Okuno, Ricky Lee*

- 16-1 **Preparation of Active Layer of Solar Cells Device by F8T2 Blending with PCBM,**
Han-Sheng Huang, Po-Yi Lu, Cho-Liang Chung and Shen-Li Fu / I-Shou University
- 16-2 **A novel polymer technology for underfill,**
Osamu Suzuki¹, Toshiyuki Sato¹, Pawel Czubarow² Tomasz Waecho² and Dave Son³ / NAMICS Corporation¹, eM-TECH, inc², Southern Methodist University³
- 16-3 **Transparent Encapsulating Resin for Automotive Applications,**
Hisataka Ito, Hiroshi Noro and Shinya Oota / NITTO DENKO Corporation
- 16-4 **High reliability epoxy encapsulating compound for power module,**
Yuya Kitagawa, Satomi Yano, Hironori Kobayashi and Aya Mizushima / NITTO DENKO Corporation

Author's Interview (20min.)

15:30 – 17:10 Session 17: Material (ML-3)

Session Chair: *Hiroshi Manita, Itsuo Watanabe*

- 17-1 **Phase Transformation of Metallic Nanoparticle Deposites for the Electrodes of Flexible Electronics,**
Tzu-Hsuan Kao², Jenn-Ming Song¹, Jian-Yih Wang¹ and In-Gann Cher² / National Dong Hwa University¹,

National Cheng Kung University²

- 17-2 **A New, Cost-effective Coreless Substrate Technology,**
Bernd K. Appelt, Bruce Su, Alex S.F. Huang and Yi-Shao Lai / ASE Group Inc.
- 17-3 **Build-up Electrical Insulation Material with Low-Dielectric Tangent, Low-CTE and Low-Surface Roughness,**
Isao Suzuki, Toshiaki Tanaka, Akihiro Uenishi, Takayuki Kobayashi, and Junnosuke Murakami / Sekisui Chemical Co. Ltd.
- 17-4 **Electroless Ni/Pd/Au Plating for Semiconductor Package Substrates -Effect of Gold Plating Combinations on Gold Wire Bonding Reliability-,**
Yoshinori Ejiri¹, Takehisa Sakurai¹, Yoshinori Arayama², Yoshiaki Tsubomatsu¹, Shuuichi Hatakeyama¹, Shigeharu Arike¹, Yukihiisa Hiroyama¹ and Kiyoshi Hasegawa¹ / Hitachi Chemical Co.Ltd.¹, Hitachi Chemical Techno Service Co., Ltd.²

Author's Interview (20min.)

Room 212

11:10 – 12:00 Session 18: Optoelectronics (OE-2)

Session Chair: Shigeru Nakagawa, Shigenori Aoki

- 18-1 **Invited : Multichannel optical modules with an SF optical connector interface,**
Hiromasa Tanobe¹, Shuichiro Asakawa¹, Masaru Kobayashi² and Junya Kobayashi¹ / NTT Corporation¹, NTT Advanced Technology Corp.²
- 18-2 **High-bandwidth optical MCM: FPGA with optical I/O on waveguide-integrated SLC,**
Masao Tokunari, Jean Benoit Héroux and Shigeru Nakagawa / IBM Japan, Ltd.

Author's Interview (10min.)

13:20 – 15:00 Session 19: Optoelectronics (OE-3)

Session Chair: Shigeru Nakagawa, Daisuke Iguchi

- 19-1 **4-Ch × 10-Gb/s chip-to-chip optical interconnections with optoelectronic packages and optical waveguide separated from PCB,**
Yutaka Takagi, Atsushi Suzuki, Toshikazu Horio, Takeshi Ohno, Toshifumi Kojima, Toshikatsu Takada, Satoshi Iio, Kazushige Obayashi and Masahiko Okuyama / NGK Spark Plug CO., Ltd.
- 19-2 **1060-nm 10-Gb/s x12-channel parallel-optical modules for optical interconnects,**
Toshinori Uemura, Yozo Ishikawa, Yoshinobu Nekado, Atsushi Izawa, Masakazu Yoshihara and Hideyuki Nasu / Furukawa Electric Co., Ltd.
- 19-3 **High Throughput On-board Parallel Optical Modules Using Multi-chip Visual Alignment Technique,**
Kenichro Yashiki¹, Takara Sugimoto², Ichiro Ogura¹ and Kazuhiro Kurata¹ / NEC Corporation¹, NEC Yamanashi Ltd.²
- 19-4 **Relationship between alignment errors of optical components and power consumption in optoelectronic devices,**
Hironobu Morita and Minoru Watanabe / Shizuoka University

Author's Interview (20min.)

15:30 – 16:45 Session 20: Optoelectronics (OE-4)

Session Chair: Shigenori Aoki, Daisuke Iguchi

- 20-1 **Polymeric multi/demultiplexers using light-induced self-written waveguides for cost-effective optical interconnection,**

Tatsuya Yamashita¹, Akari Kawasaki¹, Manabu Kagami¹, Takashi Yasuda² and Hideki Goto² / Toyota Central R&D Labs., Inc.¹, TOYOTA Motor Corporation²

- 20-2 **Soft-Lithographic Fabrication of Polymer Parallel Optical Waveguides with Graded-Index Cores for Board-Level Optical Interconnections,**

Takaaki Ishigure, Yosuke Nitta and Yusuke Sugimori / Keio University

- 20-3 **Optical Waveguide Materials with High Thermal Reliability and Their Applications for High-density Optical Interconnections,**

Tomoaki Shibata¹, Tatsuya Makino¹, Atsushi Takahashi¹, Yasunobu Matsuoka² and Tosahiki Sugawara² / Hitachi Chemical Co.,Ltd.¹, Hitachi Ltd.²

Author's Interview (20min.)

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Online registration starts on July 1, 2010. Please register online at

<http://vlsi-pkg-ws.org/>

On-site registration will be also available during the symposium.

We don't accept registration by mail or FAX.

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IEEE enrollment discount offer

IEEE will offer the Symposium attendees 50% off of IEEE and CPMT Society enrollment fee covering from September 2010 through December 2011. Enrollment form and transaction are available between 12:00 and 13:00 on Aug. 24 - 26.

Meeting attire

Business casual: No suit, No tie, No T-shirt, No Bermuda shorts.

Refrain from bringing drinks to the conference room

Please refrain from drinking or eating in a conference room.

Bringing drinks or foods into the conference room is prohibited in the University of Tokyo.

Drinks will be served outside the room during the break time.

Lunch

Lunch is available at several places in the University of Tokyo, such as Chuo refectory, Matsumoto-rou, and Subway sandwich stand.

Restraint Map in Hongo Campus is

<http://www.u-tokyo.ac.jp/campusmap/restaurantmap.pdf>

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The University of Today



Akamon (Red Gate)

The University of Tokyo was established in 1877 as the first national university in Japan. As a leading research university, the University of Tokyo offers courses in essentially all academic disciplines at both undergraduate and graduate levels and conducts research across the full spectrum of academic activity. The university aims to provide its students with a rich and varied academic environment that ensures opportunities for both intellectual development and the acquisition of professional knowledge and skills.

The University of Tokyo has a faculty of over 4,000 and a total enrollment of about 29,000, evenly divided between undergraduate and graduate students. As of 2006 there were 2,269 international students, and over 2,700 foreign researchers come annually to the university for both short and extended visits. The University of Tokyo is known for the excellence of its faculty and students and ever since its foundation many of its graduates have gone on to become leaders in government, business, and the academic world.

The University of Tokyo is composed of three campuses: Hongo, Komaba, and Kashiwa. In addition, some University of Tokyo facilities are situated in other parts of both Tokyo and the country. The main campus of the university is located in Hongo Bunkyo-ku, Tokyo and occupies about 56 hectares of the former Kaga Yashiki, the Tokyo estate of a major feudal lord. Parts of the seventeenth century landscaping of the original estate have been preserved to provide greenery and open space. The campus is graced by the Kaga Estate's celebrated Akamon, or Red Gate, which dates from 1827 and has been designated as an 'Important Cultural Property' by the Japanese Government. Most of the faculties, graduate schools, and research institutes of the university are located on the Hongo Campus



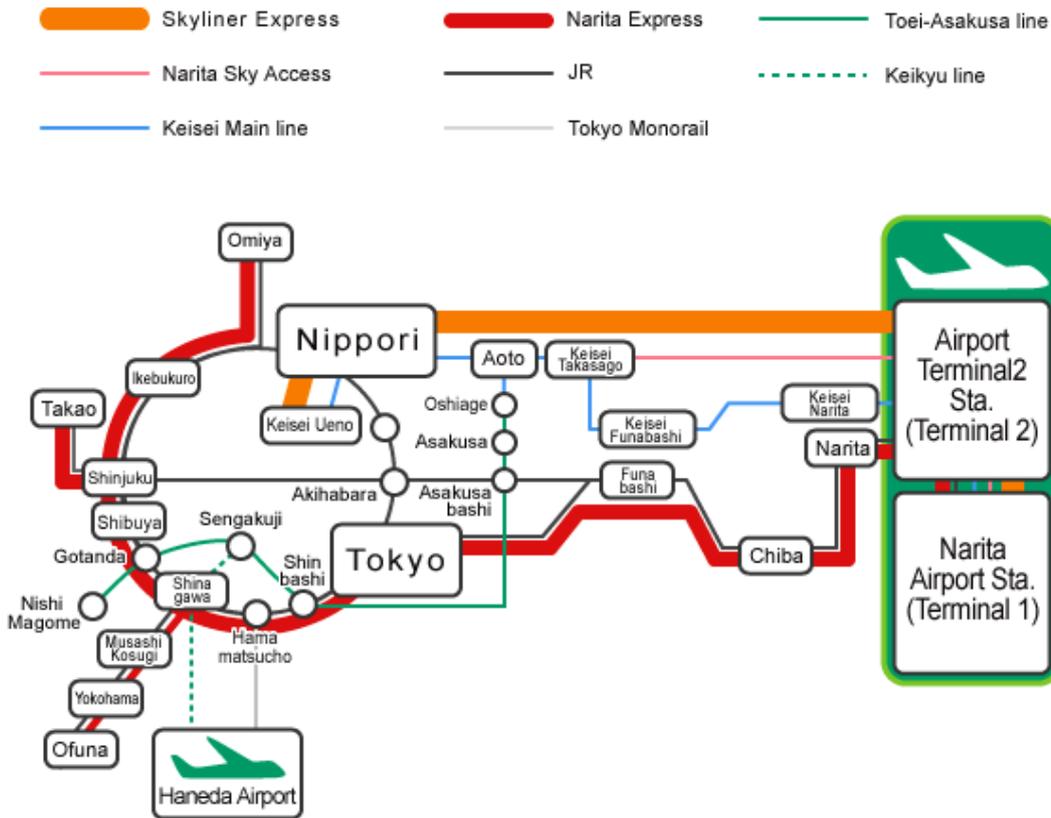
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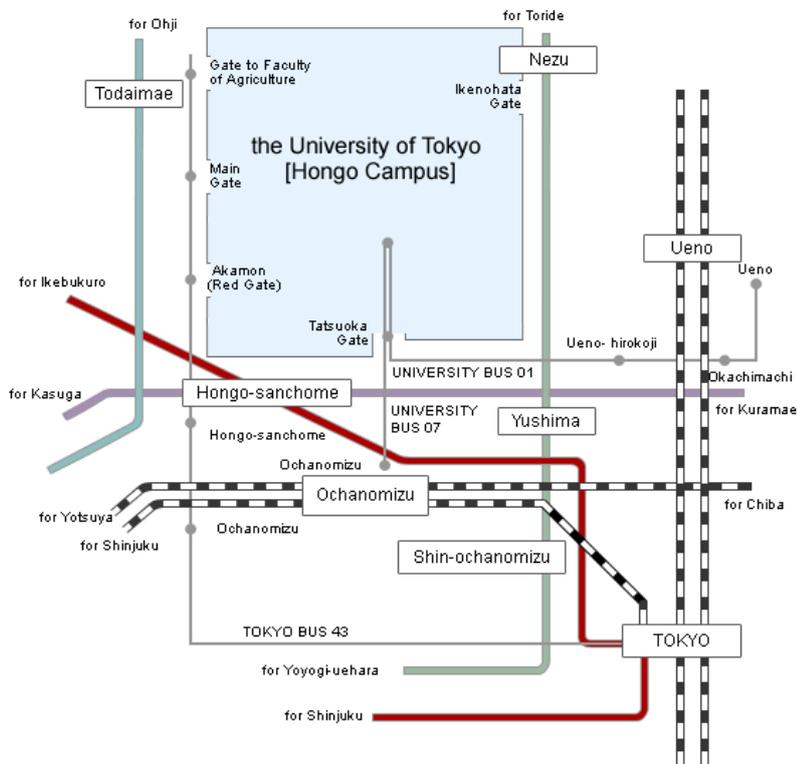
Access to the University of Tokyo, Hongo Campus

Go to nearest station from Narita Airport, use the JR or Keisei line.



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	Airport Narita (Rapid Service)		Approx. 90 min.	
Narita Sky Access	Skyliner	Keisei Ueno	Approx. 44 min.	Access guide to Narita Airport by Keisei Railway Access guide to Haneda Airport by Keikyu Railway
	Limited Express		Approx. 75 min.	
Keisei Main Line	City Liner		Approx. 74 min.	
	Morning Liner		Approx. 78 min	
	Evening Liner			
	Rapid Express		Approx. 85 min	

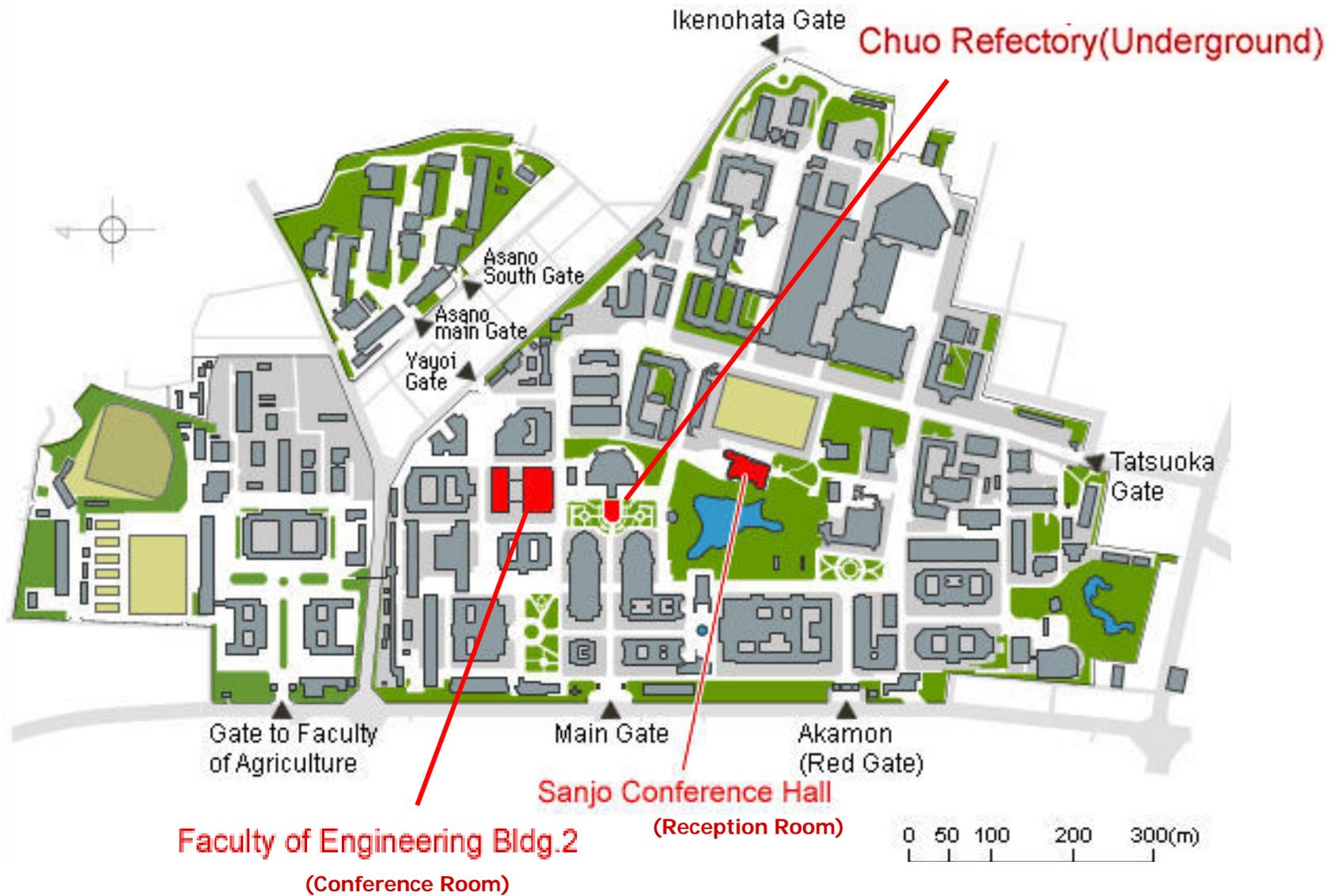
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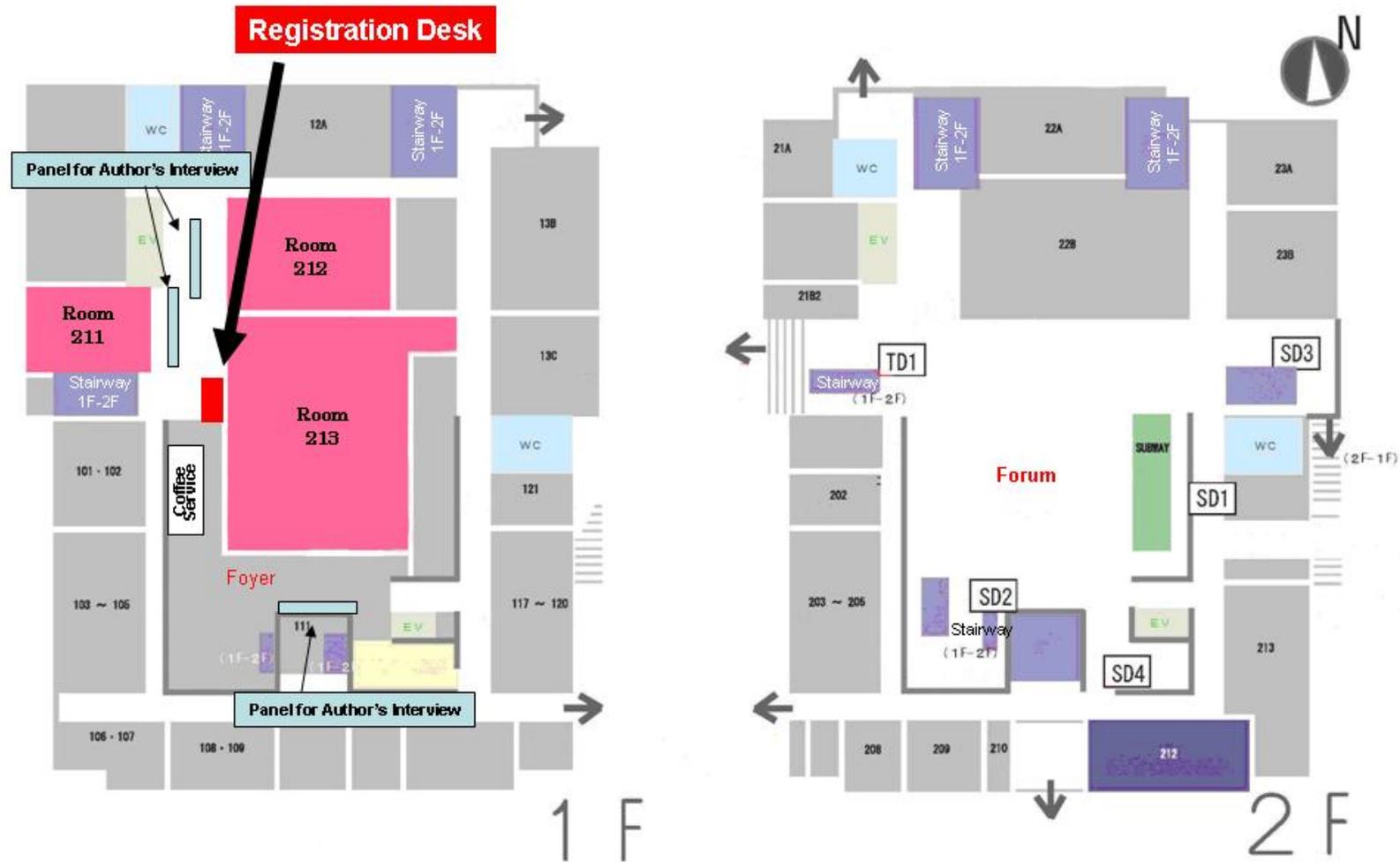
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Hongo-sanchome Station. (Subway Marunouchi Line)	8 min. walk
Hongo-sanchome Station. (Subway Oedo Line)	6 min. walk
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Todaimae Station. (Subway Namboku Line)	1 min. walk
Kasuga Station. (Subway Mita Line)	10 min. walk

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	Bus	Toei Bus 学 07 for Tokyo Univ. and get off at Todai (Tatsuokamon, Byoin-mae, Konai Bus Stop)
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Campus Map of the University of Tokyo, Hongo Campus



Faculty of Engineering Bldg. 2



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